AMENDMENTS TO THE CLAIMS:

The status of the claims is as follows:

1. (Previously Presented) A bus arbitrator comprising:

an input circuit receiving a first bus access request signal from a first bus device and a second bus access request signal from a second bus device, the input circuit outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit generating a time-delayed first bus access request signal from the first bus access request signal and a time-delayed second bus access request signal from the second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled and generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled,

wherein the second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less

than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

2. (Previously Presented) The bus arbitrator as set forth in claim 1 wherein the comparator circuit:

disables the first line driver enable signal if either of the first bus access request signal or the time-delayed first bus access request signal is disabled; and

disables the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

3. (Previously Presented) The bus arbitrator as set forth in claim 2 wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with tri-state line drivers on a shared bus.

4. (Previously Presented) The bus arbitrator as set forth in claim 3 wherein the comparator circuit comprises:

a first AND gate having a first input receiving the first bus access request signal and a second input receiving the time-delayed first bus access request signal; and

a second AND gate having a first input receiving the second bus access request signal and a second input receiving the time-delayed second bus access request signal.

5. (Previously Presented) The bus arbitrator as set forth in claim 3 wherein the delay circuit is an asynchronous delay circuit.

6. (Previously Presented) The bus arbitrator as set forth in claim 5 wherein the delay circuit comprises:

a first set of an even number of inverters connected in series, wherein a first inverter in the first set receives the first bus access request signal and a last inverter in the first set generates the time-delayed first bus access request signal; and

a second set of an even number of inverters connected in series, wherein a first inverter in the second set receives the second bus access request signal and a last inverter in the second set generates the time-delayed second bus access request signal.

7. (Previously Presented) The bus arbitrator as set forth in claim 3 wherein the delay circuit is a synchronous delay circuit.

8. (Previously Presented) The bus arbitrator as set forth in claim 7 wherein the delay circuit comprises:

a first flip-flop having an input receiving the first bus access request signal and an output coupled to the comparator circuit that generates said time-delayed first bus access request signal;

a first inverter having an input receiving the clock signal and an output coupled to a clock input of the first flip-flop;

a second flip-flop having an input receiving the second bus access request signal and an output coupled to the comparator circuit that generates the time-delayed second bus access request signal; and

a second inverter having an input receiving the clock signal and an output coupled to a clock input of the second flip-flop.

9. (Previously Presented) A shared bus system comprising:

N bus devices capable of requesting access to a shared bus;

M tristate line drivers, each of the M tristate line drivers having an input for receiving a logic bit from one of the N bus devices and an output for outputting the received logic bit to the shared bus, wherein each tristate line driver outputs the received logic bit when a line driver enable signal associated with the respective tristate line driver is enabled and an output of each

tristate line driver is put into a high-impedance state when the associated line driver enable signal is disabled;

a bus arbitrator operable to activate and de-activate the M tristate line drivers, the bus arbitrator comprising:

an input circuit capable of receiving a first bus access request signal from a first of the N bus devices and a second bus access request signal from a second of the N bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit capable of receiving the first bus access request signal and generating therefrom a time-delayed first bus access request signal, the delay circuit also capable of receiving the second bus access request signal and generating therefrom a time-delayed second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit capable of generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, the comparator circuit also capable of generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus

access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal,

wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

10. (Previously Presented) The shared bus system as set forth in claim 9 wherein the comparator circuit:

disables the first line driver enable signal if either the first bus access request signal or the time-delayed first bus access request signal is disabled; and

disables the second line driver enable signal if either of the second bus access request signal or the time-delayed second bus access request signal is disabled.

11. (Previously Presented) The shared bus system as set forth in claim 10 wherein the second delay of the delay circuit is greater than a maximum de-activation delay period associated with the tri-state line drivers.

12. (Previously Presented) The shared bus system as set forth in claim 11 wherein the comparator circuit comprises:

a first AND gate having a first input for receiving the first bus access request signal and a second input for receiving the time-delayed first bus access request signal; and

a second AND gate having a first input for receiving the second bus access request signal and a second input for receiving the time-delayed second bus access request signal.

13. (Previously Presented) The shared bus system as set forth in claim 11 wherein the delay circuit is an asynchronous delay circuit.

14. (Previously Presented) The shared bus system as set forth in claim 13 wherein the delay circuit comprises:

a first set of an even number of inverters connected in series, wherein a first inverter in the first set receives the first bus access request signal and a last inverter in the first set generates the time-delayed first bus access request signal; and

a second set of an even number of inverters connected in series, wherein a first inverter in the second set receives the second bus access request signal and a last inverter in the second set generates the time-delayed second bus access request signal.

15. (Previously Presented) The shared bus system as set forth in claim 11 wherein the delay circuit is a synchronous delay circuit.

16. (Previously Presented) The shared bus system as set forth in claim 15 wherein the delay circuit comprises:

a first flip-flop having an input capable of receiving the first bus access request signal and an output coupled to the comparator circuit that generates the time-delayed first bus access request signal;

a first inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the first flip-flop;

a second flip-flop having an input capable of receiving the second bus access request signal and an output coupled to the comparator circuit that generates the time-delayed second bus access request signal; and

a second inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the second flip-flop.

17. (Previously Presented) For use in a shared bus system comprising N bus devices capable of requesting access to a shared bus, a method for activating and de-activating a plurality of tristate line drivers coupled between the shared bus and the N bus devices, the method comprising the steps of:

receiving a first bus access request signal from a first of the bus devices;

receiving a second bus access request signal from a second of the bus devices;

blocking the second bus access request signal when the first bus access request signal is enabled, the blocking step associated with a first delay;

generating from the first bus access request signal a time-delayed first bus access request signal and generating from the second bus access request signal a time-delayed second bus access request signal, the generating step associated with a second delay;

comparing the first bus access request signal and the time-delayed first bus access request signal and generating a first line driver enable signal only if both of the first bus access request signal and the time-delayed first bus access request signal are enabled; and

comparing the second bus access request signal and the time-delayed second bus access request signal and generating a second line driver enable signal only if both of the second bus access request signal and the time-delayed second bus access request signal are enabled,

wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, and

wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

18. (Previously Presented) The method as set forth in claim 17 further comprising the steps of:

disabling the first line driver enable signal if either of the first bus access request signal and the time-delayed first bus access request signal is disabled; and

disabling the second line driver enable signal if either of the second bus access request signal and the time-delayed second bus access request signal is disabled.

19. (Previously Presented) The method as set forth in claim 18 wherein the second delay is greater than a maximum de-activation delay period associated with the plurality of tri-state line drivers.

20. (Previously Presented) The method as set forth in claim 19 wherein the comparing steps comprise using a comparator circuit, the comparator circuit comprising:

a first AND gate having a first input for receiving the first bus access request signal and a second input for receiving the time-delayed first bus access request signal; and

a second AND gate having a first input for receiving the second bus access request signal and a second input for receiving the time-delayed second bus access request signal.

21. (Previously Presented) The bus arbitrator of Claim 1, wherein the input circuit comprises:

an inverter capable of receiving and inverting the first bus access request signal; and

an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal, the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled.

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